UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Addr ss: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/352,362	07/13/99	YAMAZAKI	S 0756-1996

022204
NIXON PEABODY, LLP
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN VA 22102

MMC1/0718

EXAMINER	
DIAZ,J	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/18/01

Pleas find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Offic Action Summary	Application No. 09/352,362	Applicant(s) YAMAZAKI ET AL.	
	Examiner José R. Díaz	Art Unit 2815	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *15-26,28 and 30-87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-26,28 and 30-87* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 11 .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Double Patenting

➢ The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

➢ Claims 15-26, 28 and 30-87 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 5-35 of copending Application No. **09/352,194**. Although the conflicting claims are not identical, they are not patentably distinct from each other because the invention defined in a claim in the application is an obvious variation of the invention defined in a claim in the copending Application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

➢ Claims 15-26, 28 and 30-87 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 5-31, 45-68 and 81 of copending Application No. **09/352,373**. Although the conflicting claims are not identical, they are not patentably distinct from each other

because the invention defined in a claim in the application is an obvious variation of the invention defined in a claim in the copending Application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

➢ Claims 15-19, 20-24 and 28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of Zhang et al. (U.S. Patent No. 6,077,758) in view of Zhang et al. (U.S. Patent No. 5,529,937).

Regarding claims 15-19, Zhang et al. ('758) claim a method of manufacturing a semiconductor device (see claims 1-50) comprising the steps of: forming a catalyst element for promoting a crystallization of a non-monocrystal silicon film (i.e."amorphous semiconductor thin film"): crystallizing the non-monocrystal silicon film by thermal annealing (i.e."first heat treatment"); and performing a second crystallization (i.e."second heat treatment") in an atmosphere containing a halogen compound gas (i.e."reducing atmosphere") (See claim 1). Regarding the range of temperature claimed by Applicant, Zhang et al. ('758) define the step of the heat treatment in column 15, lines 4-17 of the disclosure as an irradiating step performed at a temperature between about 900-1200 °C.

Regarding claims 20-24, Zhang et al. ('758), as stated before, claim a method of manufacturing a semiconductor device (see claims 1-50) comprising the steps of: forming a catalyst element for promoting a crystallization of a non-monocrystal silicon film (i.e."amorphous semiconductor thin film"): crystallizing the non-monocrystal silicon film by thermal annealing (i.e."first heat treatment"); and performing a second

crystallization (i.e."third heat treatment") in an atmosphere containing a halogen compound gas (i.e."reducing atmosphere") (See claim 1). Regarding the range of temperature claimed by Applicant, Zhang et al. ('758) define the step of the heat treatment in column 15, lines 4-17 of the disclosure as an irradiating step performed at a temperature between about 900-1200 °C. However, Zhang et al. ('758) do not claim the step of carrying out a second heat treatment of irradiating the crystalline semiconductor thin film with ultraviolet light or infrared light. Zhang et al. ('937) teach performing two annealing steps in reducing atmosphere at a temperature between about 900-1200 °C after the first heat treatment is performed (See col. 9, lines 23-25 and 46-55; and col. 10, lines 2-3). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Zhang et al. ('758) to include the step of performing two annealing steps in reducing atmosphere at a temperature between about 900-1200 °C after the first heat treatment is performed. The ordinary artisan would have been motivated to modify Zhang et al. ('758) in the manner described above for at least the purpose of further promoting crystallization of the silicon film.

Regarding claims 28, Zhang et al. ('937) do not claim carrying out a second heat treatment in an atmosphere containing hydrogen. Zhang et al. ('937) teach irradiating infrared rays in an atmosphere containing H_2 at a temperature between about 900-1200 (Column 9, lines 50-51 and 54-55). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Zhang et al. ('758) to include the step of carrying out a second heat treatment in an atmosphere

containing hydrogen. The ordinary artisan would have been motivated to modify Zhang et al. ('758) in the manner described above for at least the purpose of further promoting crystallization of the silicon film.

➢ Claims 25-26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of Zhang et al. (U.S. Patent No. 6,077,758) in view of Yamazaki (U.S. Patent No. 6,197,624 B1).

Regarding claims 25-26, Zhang et al. ('758), as stated before, claim a method of manufacturing a semiconductor device (see claims 1-50) comprising the steps of: forming a catalyst element for promoting a crystallization of a non-monocrystal silicon film (i.e."amorphous semiconductor thin film"); crystallizing the non-monocrystal silicon film by thermal annealing (i.e."first heat treatment"); and performing a second crystallization (i.e."third heat treatment") in an atmosphere containing a halogen compound gas (i.e."reducing atmosphere") (See claim 1). Regarding the range of temperature claimed by Applicant, Zhang et al. ('758) define the step of the heat treatment in column 15, lines 4-17 of the disclosure as an irradiating step performed at a temperature between about 900-1200 °C. However, Zhang et al. ('758) do not claim introducing impurities of group 15 in the crystalline semiconductor thin film; and heating and patterning in the crystalline semiconductor thin film. Yamazaki, after the step of carrying out a first heat treatment, teach performing the steps of: introducing phosphorus into the crystalline semiconductor film; and heating and patterning the crystalline semiconductor thin film to form at least one crystalline semiconductor island (see col. 7, lines 54-59; and col. 8, lines 38-43). Therefore, it would have been obvious

to one having ordinary skill in the art at the same time the invention was made to modify Zhang et al. ('758) to include the step of introducing phosphorus into the crystalline semiconductor film; and heating and patterning the crystalline semiconductor thin film to form at least one crystalline semiconductor island. The ordinary artisan would have been motivated to modify Zhang et al. ('758) in the manner described above for at least the purpose of creating the active region of the TFT device.

Claim Rejections - 35 USC § 102

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

➢ Claims 15-24, 28 and 30-87 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (US Patent No. 6,077,731).

Regarding claim 15, Yamazaki et al. ('731) teaches a method of forming a TFT device (see columns 1-128) comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (see col. 63, lines 6-8); carrying out a first heat treatment (see col. 63, lines 9-20); and carrying out a second treatment at 900-1100 °C in reducing atmosphere (see col. 13, lines 41-44; and col. 63, lines 56-61).

Regarding claims 17-18 and 28, Yamazaki et al. ('731) teaches a method of forming a TFT device (see columns 1-128) comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (see col. 63, lines 6-

8); carrying out a first heat treatment (see col. 63, lines 9-20); and carrying out a second treatment at 900-1100 °C in reducing atmosphere including a halogen element (see col. 13, lines 34-44; and col. 63, lines 56-61).

Regarding claims 16 and 19, Yamazaki et al. ('731) teaches a method of forming a TFT device (see columns 1-128) comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (see col. 63, lines 6-8); carrying out a first heat treatment (see col. 63, lines 9-20); and carrying out a second treatment at 900-1100 °C in reducing atmosphere containing nitrogen and a halogen element, wherein the concentration of oxygen is not higher than 10 ppm (see col. 71, lines 66-67; col. 72, lines 1-3; and col. 77, lines 63-67).

Regarding claim 20, Yamazaki et al. ('731) teaches a method of forming a TFT device (see columns 1-128) comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (see col. 63, lines 6-8); carrying out a first heat treatment (see col. 63, lines 9-20); carrying out a second treatment with ultraviolet or infrared light (see col. 63, lines 47-50); and carrying out a third treatment at 900-1100 °C in reducing atmosphere (see col. 13, lines 41-44; and col. 63, lines 56-61).

Regarding claim 22-23, Yamazaki et al. ('731) teaches a method of forming a TFT device (see columns 1-128) comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (see col. 63, lines 6-8); carrying out a first heat treatment (see col. 63, lines 9-20); carrying out a second treatment with ultraviolet or infrared light (see col. 63, lines 47-50); and carrying out a third treatment at

900-1100 °C in reducing atmosphere including a halogen element (see col. 13, lines 34-44; and col. 63, lines 56-61).

Regarding claims 21 and 24, Yamazaki et al. ('731) teaches a method of forming a TFT device (see columns 1-128) comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (see col. 63, lines 6-8); carrying out a first heat treatment (see col. 63, lines 9-20); carrying out a second treatment with ultraviolet or infrared light (see col. 63, lines 47-50); and carrying out a third treatment at 900-1100 °C in reducing atmosphere containing nitrogen and a halogen element, wherein the concentration of oxygen is not higher than 10 ppm (see col. 71, lines 66-67; col. 72, lines 1-3; and col. 77, lines 63-67).

Regarding claims 30, 32, and 34, Yamazaki et al. ('731) teach a method of forming a TFT device (see columns 1-128) comprising the steps of: forming semiconductor film (169) (see col. 62, lines 23-25); crystallizing said semiconductor film (see col. 63, lines 9-20); etching a surface to remove an oxide (172) (see col. 65, lines 15-20); and heating said semiconductor film in inactive atmosphere (see col. 71, lines 66-67). Further, Yamasaki et al. teach that the heating said semiconductor film in inactive atmosphere is performed at a temperature of 900-1100 °C (see col. 13, lines 41-44 and col. 72, lines 10-13).

Regarding claims 31, 33, and 35 Yamazaki et al. ('731) teach a method of forming a TFT device (see columns 1-128) comprising the steps of: forming semiconductor film (169) (see col. 62, lines 23-25); crystallizing said semiconductor film (see col. 63, lines 9-20); treating a surface of said semiconductor film with hydrofluoric

to remove an oxide (172) (see col. 65, lines 15-20); and heating said semiconductor film in inactive atmosphere (see col. 71, lines 66-67). Further, Yamasaki et al. teach that the heating said semiconductor film in inactive atmosphere is performed at a temperature of 900-1100 °C (see col. 13, lines 41-44 and col. 72, lines 10-13).

Regarding claims 36-41, Yamazaki et al. ('731) teach that the heating step is carried out by furnace annealing (see col. 12, lines 66-67 and col. 13, line 1; and col. 71, lines 66-67).

Regarding claims 42-45, Yamazaki et al. ('731) teach that the heating step is carried out while exposing the semiconductor film (see col. 71, lines 63-67).

Regarding claim 46-48, 53-55, 60-62, 67-69, 74-76 and 81-83, Yamazaki et al. ('731) teach that the crystallization is performed in an inactive atmosphere or in an atmosphere containing hydrogen or oxygen (see col. 13, lines 3-6).

Regarding claims 49-52, 56-59, 63-66, 70-73, 77-80 and 84-87, Yamazaki et al. ('731) teach that the crystallization is carried out by heat treatment or by irradiating intense light such as ultraviolet ray or infrared ray (see col. 12, lines 66-67 and col. 13, lines 1-3).

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

- Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US Patent No. 6,077,731).

Regarding claims 25-26, Yamazaki et al. ('731) teaches a method of forming a TFT device (see columns 1-128) comprising the steps of: adding a catalytic element to at least a portion of the amorphous semiconductor film (see col. 63, lines 6-8); carrying out a first heat treatment (see col. 63, lines 9-20); carrying out a second treatment at 900-1100 °C in reducing atmosphere (see col. 13, lines 41-44; and col. 63, lines 56-61); patterning the crystalline semiconductor (see col. 67, lines 52-54); selectively providing the crystalline semiconductor with phosphorus (see col. 69, lines 21-22); and carrying out a third heat treatment to activate the regions into which the impurity ions have been injected (see col. 69, lines 27-28). Regarding the order of the method steps of Yamasaki et al., Applicant is advised that it would have been an obvious matter of design choice to switch steps, since the transposition of process steps or the splitting of one step into two, where the processes are substantially identical or equivalent in terms of function,

manner and result, was not held to be patentably distinguishable. Ex parte Rubin 128 USPQ 159 (PO BdPatApp1959).

Response to Arguments

➢ Applicant's arguments with respect to claims 15-26, 28, 30-87 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

➢ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Takemura (US Patent No. 5,616,506) discloses a semiconductor device having a crystallized silicon thin film.

➢ Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
July 11, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800